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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,213	04/01/2004	Judy M. Gehman	03-1002/L13.12-0246	7306
7590 LSI Logic Corporation Leo J. Peters MS D-106 1621 Barber Lane Milpitas, CA 95035	04/18/2007		EXAMINER RAMPURIA, SATISH	ART UNIT PAPER NUMBER 2191
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	04/18/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/816,213	GEHMAN ET AL.
	Examiner Satish S. Rampuria	Art Unit 2191

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 01 April 2004.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 01 April 2004 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 07/21/2004.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_

***DETAILED ACTION***

1. This action is in response to the application filed on 04/01/2004.
2. Claims 1-20 are pending.

***Information Disclosure Statement***

3. An initialed and dated copy of Applicant's IDS form 1449 filed on 07/21/2004 is attached to the instant Office action.

***Oath/Declaration***

4. The Office acknowledges receipt of a properly signed oath/declaration filed 07/21/2004.

***Specification***

5. The disclosure is objected to because of the following informalities:  
Appropriate correction is required.
6. The use of the trademark/service mark "Java" has been noted in this application (i.e., page 6). It should be appropriate or proper term (i.e., Java<sup>TM</sup>) (see MPEP 608.01(v)) used, wherever it appears and be accompanied by the generic terminology (for details please visit <http://www.sun.com/suntrademarks/index.html>). Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

***Drawings***

7. The drawings were received on 04/01/2004. These drawings are acceptable by the examiner.

***Claim Rejections - 35 USC § 101***

8. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 1-15 rejected under 35 U.S.C. 101 because the act of "coding" is merely a thought or an abstract idea and does not appear to produce a tangible result even if the step of code does occur, since the result is not conveyed in the real world. Therefore, the claims do not meet the statutory requirement of 35 U.S.C. § 101, since the claim does not produce a concrete, useful, and tangible result.

Claim 16-20 rejected under 35 U.S.C. 101 because the act of "instantiating" is merely a thought or an abstract idea and does not appear to produce a tangible result even if the step of instance does occur, since the result is not conveyed in the real world. Therefore, the claims do not meet the statutory requirement of 35 U.S.C. § 101, since the claim does not produce a concrete, useful, and tangible result.

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Therefore, the claims do not meet the statutory requirement of 35 U.S.C. § 101, since the claims are not directed to a practical application of the § 101 judicial exception producing a result tied to the physical world.

***Claim Rejections - 35 USC § 102***

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-3, 5-11, and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Publication No. 2002/0100029 to Bowen (hereinafter, Bowen).

**Per claim 1:**

Bowen discloses:

1. A method for coding a hardware description of a peripheral device for multiple instantiations within a single chip, the method comprising:  
configuring a function block to instantiate the hardware description with options associated with different configurations of the peripheral device (paragraph [009] “A function written in a C programming language is received. The C function is compiled into processor instructions, which are in turn used to generate hardware configuration information. The hardware configuration information is utilized to configure a Field Programmable Gate Array (FPGA) for compiling the function to the FPGA”); and  
selecting between the options at compile time for each instantiation of the peripheral device (paragraph [0031] “The codesign system comprising means for receiving a specification of the functionality,

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partitioning means for partitioning implementation of the functionality between (a) and (b) and for customizing the hardware and/or the machine in accordance with the selected partitioning of the functionality"); wherein the options are selected without modification to the hardware description (paragraph [0036] "a hardware compiler for producing from those parts of the specification partitioned to hardware a register transfer level description for configuring configurable logic resources").

**Per claim 2:**

The rejection of claim 1 is incorporated and further, Bowen discloses:

2. The method of claim 1 wherein the step of selecting comprises:

passing a parameter value to the function block at compile time for each instantiation of the hardware peripheral (paragraph [0109] "RTL descriptions are passed straight through to the RTL synthesizer e.g. a Handel-C compiler."); and

instantiating the peripheral device using code according to the parameter value (paragraph [0111]

"Behavioral descriptions will be scheduled in such a way that the block of code will execute within that number of cycles, when possible. An error is generated if it is not possible").

**Per claim 3:**

The rejection of claim 1 is incorporated and further, Bowen discloses:

3. The method of claim 1 wherein the configuration options are peripheral design functions, peripheral design pin widths, or peripheral design interface pin outs (paragraph [0037] "The system can include a width adjuster for setting and using a desired data word size, and this can be done at several points in the desired process as necessary").

**Per claim 5:**

The rejection of claim 1 is incorporated and further, Bowen discloses:

5. The method of claim 1 wherein the step of configuring comprises:

configuring the function block with local runtime constants adapted to be overridden individually at compile time (paragraph [0134] “hardware and software compilers 304, 306, and may be used or overridden...functions which must be supplied by its subclasses... compile method on the hardware compiler class compiles the description to hardware by converting the input description to an RTL description; the compile method on the Processor A compiler compiles a description to machine code which can run on Processor A”).

**Per claim 6:**

The rejection of claim 5 is incorporated and further, Bowen discloses:

6. The method of claim 5 wherein the step of selecting comprises

overriding selected runtime constants at compile time to select between the variable options for each instance of the peripheral device (paragraph [0134] “hardware and software compilers 304, 306, and may be used or overridden...functions which must be supplied by its subclasses... compile method on the hardware compiler class compiles the description to hardware by converting the input description to an RTL description; the compile method on the Processor A compiler compiles a description to machine code which can run on Processor A”).

**Per claim 7:**

Bowen discloses:

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7. A method for coding a reusable hardware description of a peripheral device for multiple instantiations within an integrated circuit, the method comprising:

configuring a function block to instantiate the reusable hardware description with options at compile time (paragraph [009] “A function written in a C programming language is received. The C function is compiled into processor instructions, which are in turn used to generate hardware configuration information. The hardware configuration information is utilized to configure a Field Programmable Gate Array (FPGA) for compiling the function to the FPGA” and paragraph [0241] “OOP components are reusable software modules which present an interface that conforms to an object model and which are accessed at run-time through a component integration architecture”); and

instantiating multiple instances of the peripheral device on the integrated circuit by programmatically selecting between the options at compile time for each instantiation of the peripheral device (paragraph [0031] “The codesign system comprising means for receiving a specification of the functionality, partitioning means for partitioning implementation of the functionality between (a) and (b) and for customizing the hardware and/or the machine in accordance with the selected partitioning of the functionality” and paragraph [0241] “OOP components are reusable software modules which present an interface that conforms to an object model and which are accessed at run-time through a component integration architecture”).

**Per claim 8:**

The rejection of claim 7 is incorporated and further, Bowen discloses:

8. The method of claim 7 wherein the variable options are selected without modification to the reusable hardware description (paragraph [0036] “a hardware compiler for producing from those parts of the specification partitioned to hardware a register transfer level description for configuring configurable logic resources”).

**Per claim 9:**

The rejection of claim 7 is incorporated and further, Bowen discloses:

9. The method of claim 7 wherein the step of configuring comprises:

adding one or more peripheral devices based on desired features of the reusable hardware to the integrated circuit at compile time.

**Per claim 10:**

The rejection of claim 7 is incorporated and further, Bowen discloses:

10. The method of claim 7 wherein the step of configuring comprises: instantiating peripheral devices onto the integrated circuit according to the reusable hardware description wherein each instantiation is unique based on a design parameter (paragraph [0111] “Behavioral descriptions will be scheduled in such a way that the block of code will execute within that number of cycles, when possible. An error is generated if it is not possible” and paragraph [0036] “a hardware compiler for producing from those parts of the specification partitioned to hardware a register transfer level description for configuring configurable logic resources”).

**Per claim 11:**

The rejection of claim 10 is incorporated and further, Bowen discloses:

11. The method of claim 10 wherein the design parameter comprises a signal width of the peripheral device (paragraph [0037] “The system can include a width adjuster for setting and using a desired data word size, and this can be done at several points in the desired process as necessary”).

**Per claim 13:**

The rejection of claim 7 is incorporated and further, Bowen discloses:

13. The method of claim 7 wherein the step of configuring further comprises:  
configuring the function block with parameters local in scope, the parameters adapted to be  
overridden individually at compile time (paragraph [0134] “hardware and software compilers 304, 306,  
and may be used or overridden...functions which must be supplied by its subclasses... compile method on the  
hardware compiler class compiles the description to hardware by converting the input description to an RTL  
description; the compile method on the Processor A compiler compiles a description to machine code which can run  
on Processor A”).

**Per claim 14:**

The rejection of claim 13 is incorporated and further, Bowen discloses:

14. The method of claim 13 wherein the step of selecting comprises overriding selected runtime  
constants at compile time to select between the options for each instance of the peripheral device  
(paragraph [0134] “hardware and software compilers 304, 306, and may be used or overridden...functions  
which must be supplied by its subclasses... compile method on the hardware compiler class compiles the description  
to hardware by converting the input description to an RTL description; the compile method on the Processor A  
compiler compiles a description to machine code which can run on Processor A”).

**Per claim 15:**

The rejection of claim 7 is incorporated and further, Bowen discloses:

15. The method of claim 7 wherein the step of configuring comprises:

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passing a parameter value to the function block at compile time for each instantiation of the peripheral device (paragraph [0109] “RTL descriptions are passed straight through to the RTL synthesizer e.g. a Handel-C compiler”); and instantiating the peripheral device using the reusable hardware description according to the parameter value (paragraph [0111] “Behavioral descriptions will be scheduled in such a way that the block of code will execute within that number of cycles, when possible. An error is generated if it is not possible”).

**Claims 16-20** are the method claim corresponding to method claims 1, 2, 5, 6, and 11 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1, 2, 5, 6, and 11 respectively, above, as noted above.

#### ***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 4 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Bowen in view of US Patent No. 6,829,754 to Yu et al. (hereinafter, Yu).

#### **Per claim 4:**

The rejection of claim 1 is incorporated and further, Bowen does not explicitly discloses tying strap pins to power or ground.

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However, Yu discloses in an analogous computer system tying strap pins to power or ground (col. 11, lines 2-5 "Straps do not have a minimum width, defined as the width of the power pin the strap is connecting to. If the strap is smaller than the power pin it connects, a warning will be issued").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of tying strap pins to power or ground as taught by Yu into the method of using a computer program to reconfigure the logic devices as taught by Bowen. The modification would be obvious because of one of ordinary skill in the art would be motivated to strap the power or ground pins so that the power related problems can be avoided (col. 2, lines 8-11).

**Per claim 12:**

The rejection of claim 7 is incorporated and further, Bowen does not explicitly disclose defining further the function block by tying strap pins to ground or to power.

However, Yu discloses in an analogous computer system defining further the function block by tying strap pins to ground or to power (col. 11, lines 2-5 "Straps do not have a minimum width, defined as the width of the power pin the strap is connecting to. If the strap is smaller than the power pin it connects, a warning will be issued").

The feature of defining further the function block by tying strap pins to ground or to power would be obvious for the reasons set forth in the rejection of claim 4.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday except every other Friday and Wednesday and federal holidays. Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wei Y. Zhen** can be reached on **(571) 272-3708**. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria  
Patent Examiner/Software Engineer  
Art Unit 2191

*Satish S. Rampuria*  
*Patent Examiner*  
*4-16-2007*